MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering

6.331 Advanced Circuit Techniques

Spring Term 2002 — Issued : February 8, 2002
Problem Set 2 — Due : Friday, February 15, 2002

Problem 1 Consider the sample-and-hold circuit shown below.

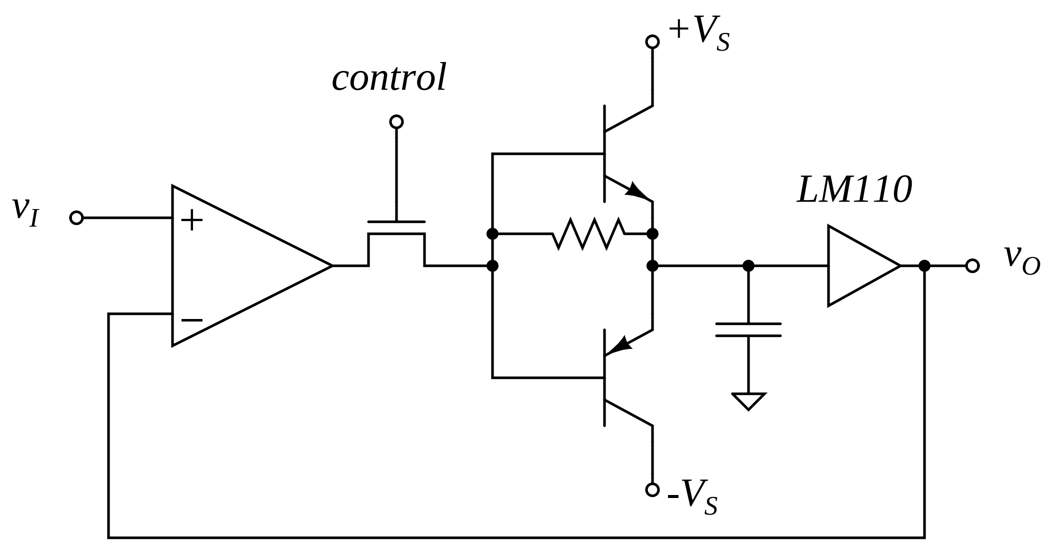

Figure 2.1: Sample and Hold Circuit

The open-loop transfer function of the op amp is

$$A(s) = \frac{10^5}{(0.01s + 1)(5(10^{-8})s + 1)^2}$$

and the closed-loop bandwidth of the LM110 amplifier is in excess of 20 MHz. The sum of the FET on resistance and the resistor shunting the current-booster transistors is 1 kΩ, and the capacitor value is 1 μF. Investigate the stability of this system under small-signal conditions of operation. Suggest a circuit modification that can be used to improve stability. Comment of the effectiveness of your method under large-signal conditions (with the booster transistors conducting) as well as for linear-region operation.

Problem 2 It was mentioned in class that the real part of the input impedance of a capacitively loaded emitter follower can be negative. Demonstrate this possibility by calculating the incremental input impedance for the connection shown.

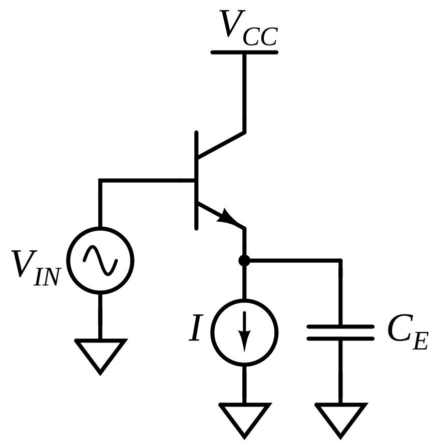

Figure 2.2: Capacitively Loaded Emitter Follower Circuit

Use a simplified incremental model for the transistor, including only r_π, c_π, and g_m.

Also show that for sufficiently large values of C_E, the real part of the input resistance will be positive at all frequencies, and determine the critical value for C_E in terms of transistor parameters.

Sketch plots of the magnitude and phase of Z_{in} for the two cases where C_E is larger and smaller than the critical value determined above.

Problem 3 Consider the problem of minimizing the additive error of a very fast sampler with a long hold time by "ganging-up" a series of sample and holds. For example using a τ_H/τ_S quotient of ten, the first sampler has a sample time of one nanosecond and a hold time of 10ns, the second sampler has $\tau_S = 10$ns and $\tau_H = 100$ns, etc.

Assume that the error of each stage is dominated by hold-time droop, and that it is proportional to the τ_H/τ_S quotient of each stage.

Assume we want a sample time of one nanosecond and a hold time of one second. What is the optimum τ_H/τ_S quotient? How many sample and holds will we need?