Recitation 13: Propagation Delay, NAND/NOR Gates

Outline

- Propagation Delay for CMOS Inverters
- Why NAND Gate is preferred over NOR Gate?
- Design Project

Propagation Delay for CMOS Inverters

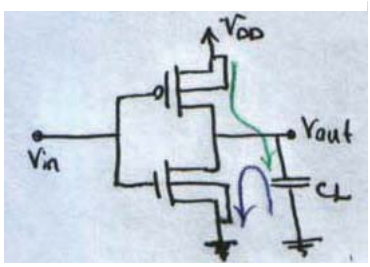


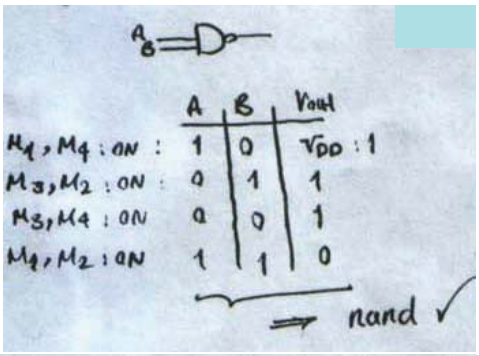
Figure 1: Discharging cycle: t_{PHL}, Charging cycle: t_{PLH}

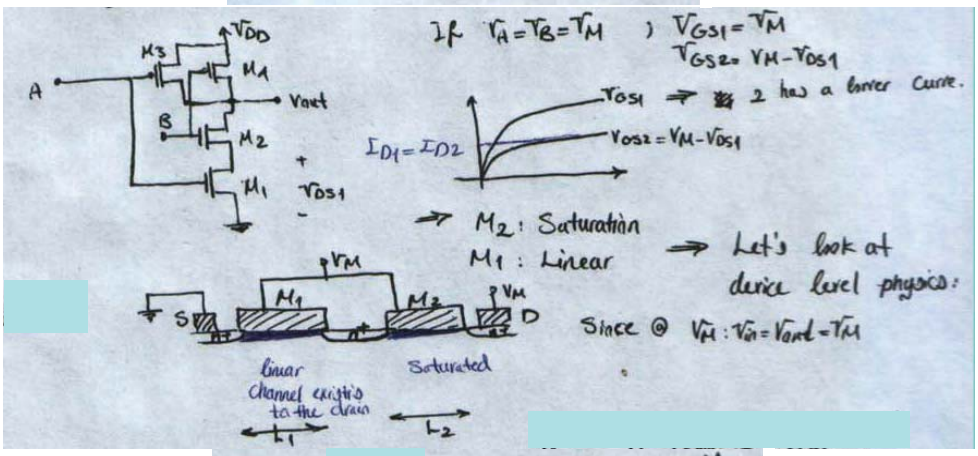
$$
\begin{aligned}
\text{Propagation time} &= \frac{1}{2}(t_{\mathrm{PLH}} + t_{\mathrm{PHL}}) \\
t &= \frac{\text{Charge(tobecharged/discharged)}}{\text{(Charging/Discharging)Current}}; \quad \text{we treat } C_{\mathrm{L}} \text{ as a linear constant capacitor} \\
t_{\mathrm{PLH}} &= \text{? charging through PMOS} \\
t_{\mathrm{PLH}} &= \frac{\frac{1}{2}C_{\mathrm{L}}V_{\mathrm{DD}}}{\frac{w_{\mathrm{p}}}{2L_{\mathrm{p}}\mu_{\mathrm{p}}C_{\mathrm{ox}}(V_{\mathrm{DD}}+V_{\mathrm{T_p}})^2}} \\
\text{why } \tfrac{1}{2}\text{?} &\quad t_{\mathrm{p}} \text{ is the time to discharge half of initial } Q \text{ or charge half of final } Q \\
t_{\mathrm{PHL}} &= \text{? discharging through NMOS} \\
t_{\mathrm{PHL}} &= \frac{\frac{1}{2}C_{\mathrm{L}}V_{\mathrm{DD}}}{\frac{w_{\mathrm{n}}}{2L_{\mathrm{n}}}\mu_{\mathrm{n}}C_{\mathrm{ox}}(V_{\mathrm{DD}}-V_{\mathrm{T_n}})^2} = \frac{C_{\mathrm{L}}V_{\mathrm{DD}}}{k_{\mathrm{n}}(V_{\mathrm{DD}}-V_{\mathrm{T_n}})^2}
\end{aligned}
$$

As seen, $t_{\mathrm{p}} \propto \mathrm{L}$. This means, the longer the devices, the slower they become. This gets us to why NAND gates are preferred.

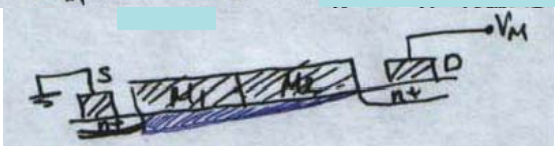
NAND vs. NOR

Gets us to why NAND gates are preferred:





This is exactly like the following:



n+ region is highly doped no resistance

Effective length of two n-channel devices in series

$$L_{\text{eff}} = 2L_{\text{n}}$$

For symmetrical transfer characteristics,

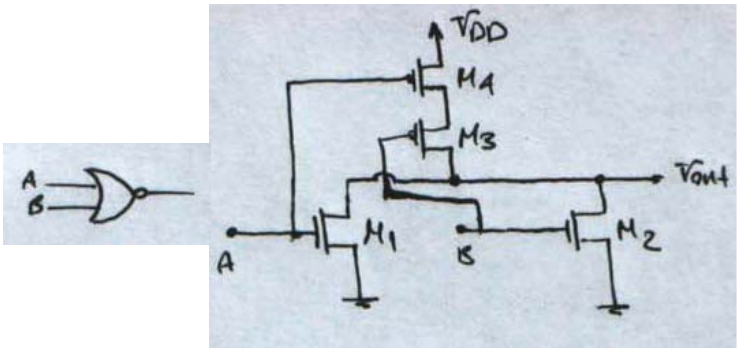
$$\begin{aligned} t_{\text{PLH}} &= t_{\text{PHL}} \\ \mu_{\text{n}} &= 2\mu_{\text{p}} \\ L_{\text{eff}_{\text{n}}} &= 2L_{\text{p}} \\ \therefore w_{\text{n}} &= w_{\text{p}} \end{aligned}$$

But since $\mu_{\text{n}} = 2\mu_{\text{p}}$, we are better off having the series connection in NAND (rather than

NOR where PMOS's are in series). If we wanted the same thing in NOR:

$$\begin{aligned} \mu_{\mathrm{n}} &= 2\mu_{\mathrm{p}} \\ L_{\mathrm{eff_p}} &= 2L_{\mathrm{eff_n}} \\ \therefore w_{\mathrm{p}} &= 4w_{\mathrm{n}} \end{aligned}$$

NOR Structure



So for NAND:

$$\left(\frac{w}{L}\right)_{\mathrm{n}} = \left(\frac{w}{L}\right)_{\mathrm{p}} \quad \text{Reason is?}$$

For M-input NAND:

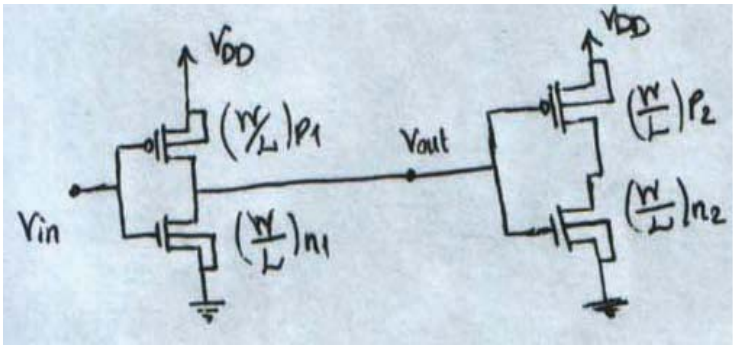
$$\left(\frac{w}{L}\right)_{\mathrm{n}} = \frac{M}{2}\left(\frac{w}{L}\right)_{\mathrm{p}}$$

M-input NAND has M-NMOS's in series $\implies L_{\mathrm{eff}} = ML_{\mathrm{n}}$. So, for $k_{\mathrm{n_{eff}}} = k_{\mathrm{p_{eff}}}$:

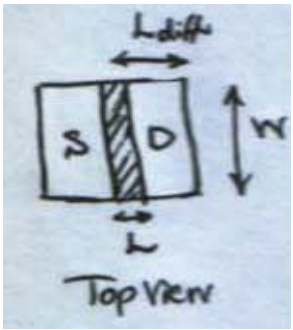
$$\begin{aligned} \frac{w_{\mathrm{n}}}{ML_{\mathrm{n}}} \times \mu_{\mathrm{n}} &= \frac{w_{\mathrm{p}}}{L_{\mathrm{p}}}\mu_{\mathrm{p}} \\ \mu_{\mathrm{n}} &= 2\mu_{\mathrm{p}} \\ \frac{w_{\mathrm{n}}}{ML_{\mathrm{n}}} \times 2 &= \frac{w_{\mathrm{p}}}{L_{\mathrm{p}}} \\ \left(\frac{w_{\mathrm{n}}}{L}\right)_{\mathrm{n}} &= \frac{M}{2}\left(\frac{w}{L}\right)_{\mathrm{p}} \end{aligned}$$

$C_{\mathrm{L}} = ?$

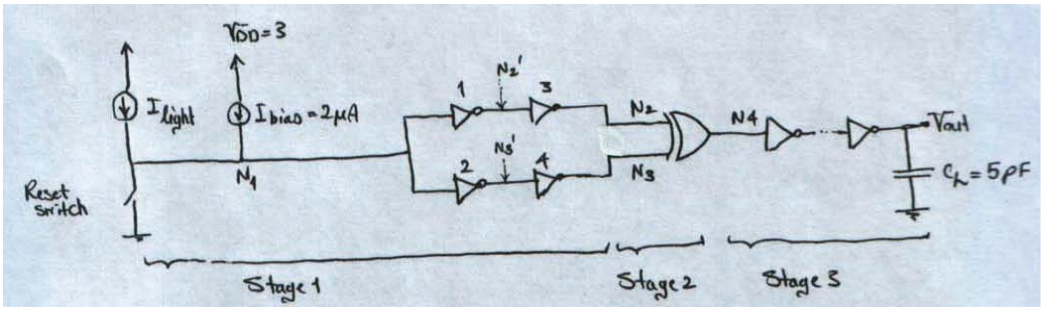
Assume the next stage is another inverter. C_{L} is all capacitances seen at node V_{out}.



$$
\begin{aligned}
C_{\mathrm{L}} &= C_{\mathrm{g_{stage2}}} + C_{\mathrm{db_{p1}}} + C_{\mathrm{db_{n1}}} \\
C_{\mathrm{g_{stage2}}} &= C_{\mathrm{g_{p2}}} + C_{\mathrm{g_{n2}}} \\
C_{\mathrm{g_{n2}}} &= \frac{2}{3} C_{\mathrm{ox}} (wL)_{\mathrm{n2}} + C_{\mathrm{ox}} w_{\mathrm{n2}} \\
&\approx C_{\mathrm{ox}} (wL)_{\mathrm{n2}} \\
C_{\mathrm{db_M}} &= C_{\mathrm{j_{n1}}} (wL_{\mathrm{diff}})_{\mathrm{n1}} + C_{\mathrm{jsw_{n1}}} (w + 2L_{\mathrm{diff}})_{\mathrm{n1}} \\
\Longrightarrow C_{\mathrm{L}} &= C_{\mathrm{ox}} (wL)_{\mathrm{n2}} + C_{\mathrm{ox}} (wL)_{\mathrm{p2}} + C_{\mathrm{j_{n1}}} (wL_{\mathrm{diff}})_{\mathrm{n1}} + C_{\mathrm{jsw_{n1}}} (w + 2L_{\mathrm{diff}})_{\mathrm{n1}} + \\
&\quad C_{\mathrm{j_{p1}}} (wL_{\mathrm{diff}})_{\mathrm{p1}} + C_{\mathrm{jsw_{p1}}} (w + 2L_{\mathrm{diff}})_{\mathrm{p1}}
\end{aligned}
$$



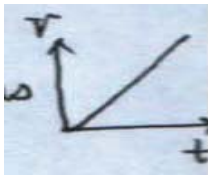
Design Project



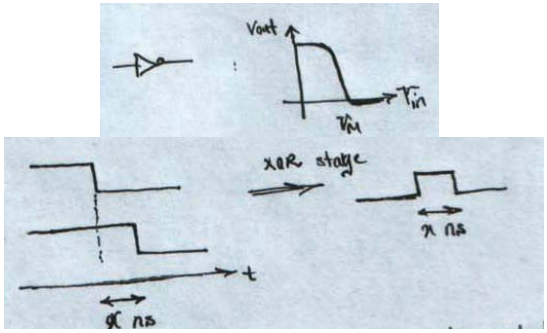
What is the use of the circuit? Light in $\Longrightarrow$ width modulated electrical signal out.

What does each stage do?

- N_1: charging 1,2 capacitors with $I_{\text{light}} + I_{\text{bias}}$



- At T_{M}: tipping point, V_{out} changes from High to Low



$$\Longrightarrow \quad \text{say } V_{\text{M},1} = 1\,\text{V}$$
$$V_{\text{M},2} = 2\,\text{V}$$

- Final stage: driver stage
  You need enough current to be able to charge C_{L} quickly enough to meet t_{r} and t_{f} of specs. Decide how many stages you need (remember V_{out} positive pulse we need), and think about ratio of sizing between stages (hint: between $3-6$ is the answer)

Specifications

- V_{out} : $t_{\text{r}}, t_{\text{f}} 3\,\text{ns}$
- Minimum gate areas
- At least 20 ns distinction between pulse widths corresponding to different I_{light} levels of $0, 1, 2, 3, \mu\text{A}$
- Report: what should you submit

Q & A about design problem

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